Amendments to the Claims

Please cancel Claims 1, 27-33 and 35-42. Please amend Claims 2, 44 and 45. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (Canceled)

2. (Currently Amended) A pipeline processor comprising:

a plurality of processing elements arranged in a serial array, each processing element having a forward processing path and a reverse processing path; and,

a clock distribution circuit in electrical communication with each processing element, a clock signal propagated along the clock distribution circuit arrives at each processing element delayed relative to the clock signal arriving at a preceding processing element data processed by a processing element in the forward processing path being gated into an adjacent processing element by the delayed clock signal received by the adjacent processing element at least a clock cycle after data is gated into the processing element ~~The pipeline processor of claim 1,~~ wherein the reverse processing path in each processing element has a process time shorter than the process time of the forward processing path.

3. (Previously Presented) The pipeline processor of claim 2 wherein the clock signal is distributed independently to each processing element.

4. (Previously Presented) The pipeline processor of claim 3 wherein the delay between any two adjacent processing elements is approximately a same delay.

5. (Previously Presented) The pipeline processor of claim 4 wherein the direction of propagation of the clock signal is switchable.

6. (Canceled)

7. (Previously Presented) The pipeline processor of claim 2 wherein the clock signal is gated from a preceding processing element to a next processing element.

8. (Previously Presented) The pipeline processor of claim 7 wherein the direction of propagation of the clock signal is switchable.

9. (Previously Presented) The pipeline processor of claim 2 wherein at least a processing element of the serial array is time-synchronized to an external circuit.

10. (Previously Presented) The pipeline processor of claim 9 wherein the external circuit includes a memory buffer.

11. (Previously Presented) The pipeline processor of claim 10 wherein the external circuit includes an input/output port for receiving data from an external data source and for providing said data to the memory buffer.

12. (Previously Presented) The pipeline processor of claim 11 wherein the serial array comprises:

a first pipeline array having a first predetermined number of processing elements, n; and,

a second different pipeline array having a second predetermined number of processing elements, m.

13. (Previously Presented) The pipeline processor of claim 12 wherein at least a processing element of the first pipeline array is in electrical communication with the memory buffer via a hardware connection, the at least a processing element of the first pipeline array being time-synchronized to the memory buffer for retrieving data therefrom.

14. (Previously Presented) The pipeline processor of claim 13 wherein the at least a processing element of the first pipeline array is a first processing element of the first pipeline array.

15. (Previously Presented) The pipeline processor of claim 13 wherein the nth element of the first pipeline array and the mth element of the second pipeline array are in electrical communication via a hardware connection, such that data having been provided to the first processing element of the first pipeline array and propagated to the nth processing element thereof is further propagated to the mth processing element of the second pipeline array for additional processing therein.

16. (Previously Presented) The pipeline processor of claim 15 wherein the first predetermined number of processing elements, n, and the second predetermined number of processing elements, m are a same predetermined number of processing elements and wherein, in use, the delay to the nth element and to the mth element is approximately equal such that a tail-to-head data transfer between the nth element of the first pipeline array and the mth element of the second pipeline array is substantially time-synchronized.

17. (Previously Presented) The pipeline processor of claim 13 wherein at least a processing element of the second pipeline array is in electrical communication with the memory buffer via a second hardware connection, the at least a processing element of the second pipeline array being time-synchronized to the memory buffer for retrieving data therefrom.

18. (Previously Presented) The pipeline processor of claim 17 wherein the at least a processing element of the second pipeline array is a first processing element of the second pipeline array.

19. (Previously Presented) The pipeline processor of claim 17 wherein the nth element of the first pipeline array and the mth element of the second pipeline array are in electrical

communication via a hardware connection, such that data having been provided to the first processing element of the first pipeline array and propagated to the nth processing element thereof is further propagated to the mth processing element of the second pipeline array for additional processing therein.

20. (Previously Presented) The pipeline processor of claim 17 comprising a third pipeline array having a third predetermined number of processing elements, q.

21. (Previously Presented) The pipeline processor of claim 20 wherein at least a processing element of the third pipeline array is in electrical communication with the memory buffer via a third hardware connection, the at least a processing element of the second pipeline array being time-synchronized to the memory buffer for retrieving data therefrom.

22. (Previously Presented) The pipeline processor of claim 21 wherein the at least a processing element of the third pipeline array is a first processing element of the third pipeline array.

23. (Previously Presented) The pipeline processor of claim 21 wherein the nth element of the first pipeline array and the mth element of the second pipeline array are in electrical communication via a first hardware connection, and the first element of the second pipeline array and the first element of the third array are in electrical communication via a second hardware connection, such that that a tail-to-head data transfer between the nth element of the first pipeline array and the mth element of the second pipeline array is substantially time-synchronized and such that a head-to-tail data transfer between the first element of the second pipeline array and the first element of the third pipeline array is substantially time-synchronized.

24. (Previously Presented) The pipeline processor of claim 12 comprising a third pipeline array having a third predetermined number of processing elements, q.

25. (Previously Presented) The pipeline processor of claim 24 wherein the nth element of the first pipeline array and mth element of the second pipeline array are in electrical communication via a first hardware connection, and the first element of the second pipeline array and the first element of the third array are in electrical communication via a second hardware connection.

26. (Previously Presented) A processing element for use in a pipeline processor comprising:

a first port for receiving a first clock signal, the first clock signal being propagated in a forward direction in the pipeline processor;

a second port for receiving a second other clock signal, the second other clock signal propagated in a reverse processing path in the pipeline processor;

a switch operable between two modes for selecting one of the first clock signal and the second other clock signal; and

wherein the selected one of the first clock signal and the second other clock signal is provided to the processing element.

27-33 (Canceled)

34. (Canceled)

35-42 (Canceled)

43. (Canceled)

44. (Currently Amended) The pipeline processor of claim [[1]] 2, wherein along the forward processing path more than one full clock cycle elapses between gating data into the processor element and gating the processed data from the processor element into the adjacent processor element.

45. (Currently Amended) The pipeline processor of claim [[1]] 2, wherein along the ~~return~~ reverse processing path less than one full clock cycle elapses between gating data into the processor element and gating the processed data into the adjacent processor element.